Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHANDRASHEKHAR S. PATWARDHAN, JAMES EARL WHITE, RICHARD BRUNNER, YAN XU, and KENNETH GRIESSER

Appeal No. 2002-2195
Application No. 08/988,616

ON BRIEF

Before JERRY SMITH, FLEMING, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 60-76, which are all the claims remaining in the application.

We affirm.

BACKGROUND

The invention is directed to a method for accessing data in a microcode ROM in a microprocessor for the purpose of checking for memory faults. Representative claim 60 is reproduced below.

> 60. A method for reading data from a microcode ROM in a microprocessor, the method comprising:
>
> invoking an instruction fetch to retrieve data from a predetermined address in the microcode ROM; and
>
> suppressing execution of the data retrieved from the predetermined address in the microcode ROM in response to a signal indicating a test mode, regardless of whether the data retrieved comprises a branch or non-branch instruction.

The examiner relies on the following reference:

Sawase et al. (Sawase)	5,175,840	Dec. 29, 1992

Claims 60-76 stand rejected under 35 U.S.C. § 102 as being anticipated by Sawase.

We refer to the Final Rejection (Paper No. 27) and the Examiner's Answer (Paper No. 31) for a statement of the examiner's position and to the Brief (Paper No. 30) for appellants' position with respect to the claims which stand rejected.

OPINION

In accordance with appellants' proposed grouping of the claims (Brief at 7), we select claims 60 and 67 as representative of the invention. See 37 CFR § 1.192(c)(7).

Appellants assert, in response to the section 102 rejection over Sawase, that the reference fails to teach "invoking an instruction fetch to retrieve data from a predetermined address in the microcode ROM," as set forth in instant claim 60. According to appellants, Sawase does not disclose or suggest any method or apparatus that uses an instruction fetch mechanism to read data from a predetermined location in the EEPROM. Appellants allege, further, that it is not possible for the EEPROM test circuit as disclosed in Sawase to invoke any instruction fetch from the CPU because only the EEPROM module is operative during the testing, and isolated from the CPU, RAM, and ROM. (Brief at 11.)

The examiner responds that instant claim 60 does not require that the instruction fetch invocation be from a CPU. The examiner finds that the claimed "invoking an instruction fetch" is taught by the data read-out occurring in response to control signals provided from outside the semiconductor circuit, pointing to column 3, lines 28 through 31 of the reference. (Answer at 5.)

Instant claim 60 does not specify the mechanism that invokes the instruction fetch, nor the location of the mechanism. We are not persuaded of error in the examiner's position. In particular, appellants have not shown why the read operation described in column 3 of Sawase, although retrieving data from a predetermined address in the EEPROM, must be considered different from the claimed step of invoking an instruction fetch to retrieve the data.

We also consider appellants' arguments at pages 12 through 15 of the Brief as failing to show error in the examiner's position with respect to the second step of instant claim 60. There appears to be no dispute that the reference teaches that EEPROM module 9 (Fig. 2) is isolated from the CPU, RAM, and ROM during testing. See Sawase col. 3, ll. 9-12. Instant claim 60 does not specify how, or by what means, execution of the data is suppressed, other than that the suppressing is "in response to a signal indicating a test mode." As described at column 3 of Sawase, when the test control signals are applied to test circuit 8 (Fig. 1), data from EEPROM matrix 10 is read out by an external structure via test I/O data buffer 18 (Fig. 2). The retrieved data is not executed by CPU 2, which is isolated from the EEPROM during test mode. Nor, for that matter, is the retrieved data executed by the external test instruments, since during test mode the EEPROM is checked for integrity of stored data, rather than serving as a source for executable instructions. In short, the data retrieved during the test mode is not executed in any case. We agree with the examiner that Sawase teaches not executing, and thus fairly teaches suppressing execution, of the retrieved data.

Instant claim 67 is narrower than claim 60 in requiring that "the microprocessor suppresses execution of the data retrieved." Appellants' arguments (Brief at 17-18) appear to equate CPU 2 of Sawase (Fig. 1) with a "microprocessor" within the meaning of the claim. However, consistent with the preamble of claim 67 and with the disclosure of Sawase, the "microprocessor" consists of more than a CPU. All the circuitry shown on substrate 1 in Sawase, including that which ensures that EEPROM module 9 is

isolated from CPU 2 during the test mode, is fairly considered a "microprocessor" within the meaning of instant claim 67. Although Sawase refers to substrate 1 as a "microcomputer," the word is, broadly speaking, synonymous with "microprocessor." See, e.g., Webster's Ninth New Collegiate Dictionary at 750 (1990) ("microcomputer... 1 : a very small computer that uses a microprocessor to handle information 2 : MICROPROCESSOR"). We thus agree with the examiner that the "wherein" clause of the claim is met by Sawase.

We appreciate the differences between appellants' invention as disclosed and the disclosure of Sawase. However, the claims measure the invention. SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc). During prosecution, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. See In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550 (CCPA 1969).

We sustain the rejection of claims 60-76 under 35 U.S.C. § 102 as being anticipated by Sawase. We have considered all of appellants' arguments, but are not persuaded that the examiner's finding of anticipation is in error. Arguments that appellants could have presented, but chose not to rely upon, are deemed waived. See 37 CFR § 1.192(a) ("Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good

cause is shown.") and § 1.192(c)(8)(iii) (the brief must point out the errors in the rejection).

CONCLUSION

The rejection of claims 60-76 under 35 U.S.C. § 102 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JERRY SMITH Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

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